

Strip Tests at CERN

- FEM #1, fem2jmd #2, SVX chain #2.
 - Power: AVDD&DVDD are from FEM. For module #2 turn-on current = 0.495A, after FPGA configuration – 0.418A, after SVX configuration – 0.470A
 - Ground: AGND&DGND are grounded at FEM
 - VCAL: 0.1V

Config file:

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----- Beginning of chip1 -----
----- Front end Bit Assignments -----
#0:127 Mask[127:0] Cal mask or channel disable register
#01234567890123456789012345678901234567890123456789
# chip disabled
# 111111111111111111111111111111111111111111111111111111111
# 111111111111111111111111111111111111111111111111111111111
# 111111111111111111111111111111111111111111111111111111111
# every 8th/9th channel
00000001000000001000000100000000100000010000000010
00000100000000100000010000000010000001000000001000
0001000000001000000100000000
# no calibrations
# 000000000000000000000000000000000000000000000000000000000
# 000000000000000000000000000000000000000000000000000000000
# 000000000000000000000000000000000000000000000000000000000
# some masked channels center of the sensor
# 10101010101010101010101010101010101010101010101010
# 10101010101010101010101010101010101010101010101010
# 10101010101010101010101010
# some masked channels, edges of the sensor
# 0101010101010101010101010101010101010101010101010101
# 0101010101010101010101010101010101010101010101010101
# 0101010101010101010101010101010101010101010101010101
#128 spare
0
#129 VCAL. Connects VCAL pad to internal voltage divider
# it has to be 1 for StripCAR1
1
#130 Disable. Mask reg act as channel disable 1 or cal mask reg 0
0
#131:134 BW[0:3]. Preamp risetime adjustment.
# 0010 090609
0000
#135:138 Isel[0:3]. Preamp input FET bias current adjustment
1010
#139:140 IWsel[0:1]. Pipeline write amp bias current adj
10
#141:142 IRsel[0:1]. Pipeline read amp bias current adj
10
#143:148 PickDel[0:5]. Trigger latency. It corresponds to JRI
# 101000

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101000
#149 PB Pipeline readout order; 0=pedestal,signal, 1=signal,pedestal
0
----- Back end bit Assignments -----
#150:156 ID[6:0]
0000001
#157 RTPS. Real Time Pedestal Subtraction disable
1
#158 Rd127. Always readout ch.127 regardless of hit status
1
#159 Rd63. Always readout ch.63 regardless of hit status
1
#160 RdAll Allways readout all channels
1
#161 RdNeigh Readout hit channels and their neighbors
1
#162:165 RampPed[0:3] ADC ramp pedestal setting
# 1001
1001
#166 RampDir ADC ramp direction; 0=ramp up
0
#167 CompPol Comparator polarity;
0
#168:170 RampRng[0:2] ADC ramp range, adjusts slope of ramp
# 111 before 071213----- Beginning
# 100 before 090427
111
#171:178 Thresh[7:0]
00000001
#179:186 CntrMod[7:0] Counter modulo. Gray code.
10000000
#187 FC First Chip flag; enables the first chip to drive ODBV
# This is irrelevant which is first or last when PriIn is
# applied.
0
#188 LC Last Chip flag; enables the last chip to drive ODBV
0
#189:191 DriverI[2:0] Output driver current select
# 000 to disable output from this chip
111
----- End of chip1 -----

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Bit stream

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0   0: 0000000100000000100000010000000010000001000000001000000100000000
0   64: 1000000100000000100000010000000010000001000000001000000100000000
0 128: 010000010101010100000000001111110010011100000001100000000111

```

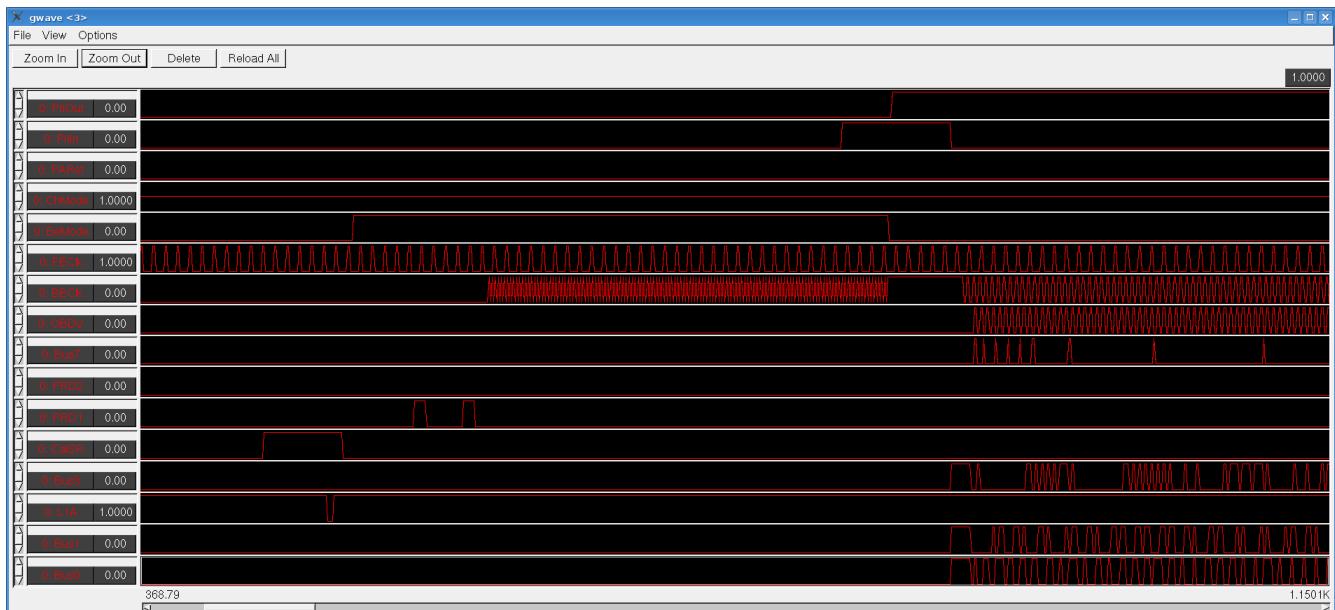


Fig. 1: SVX signal diagram

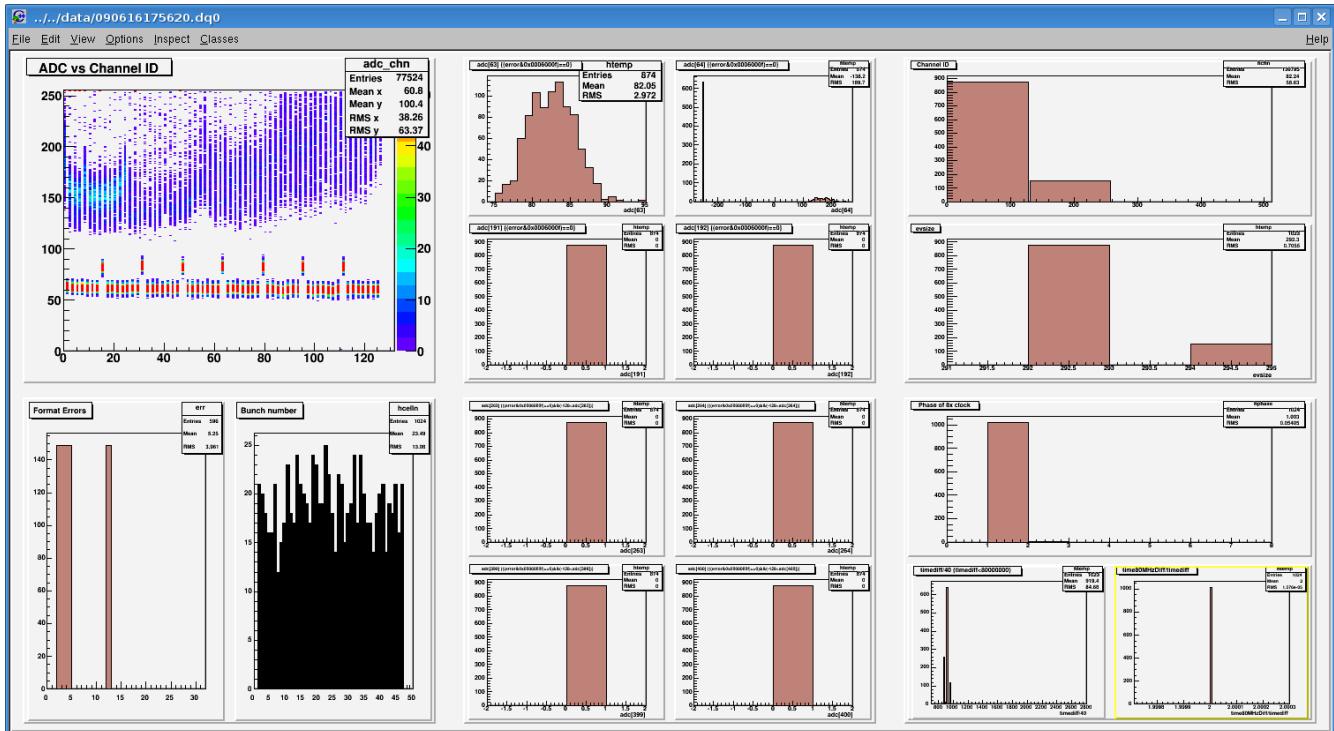


Fig. 2: Test module #2, only central wires (upper layer on the chip) are wire bonded.

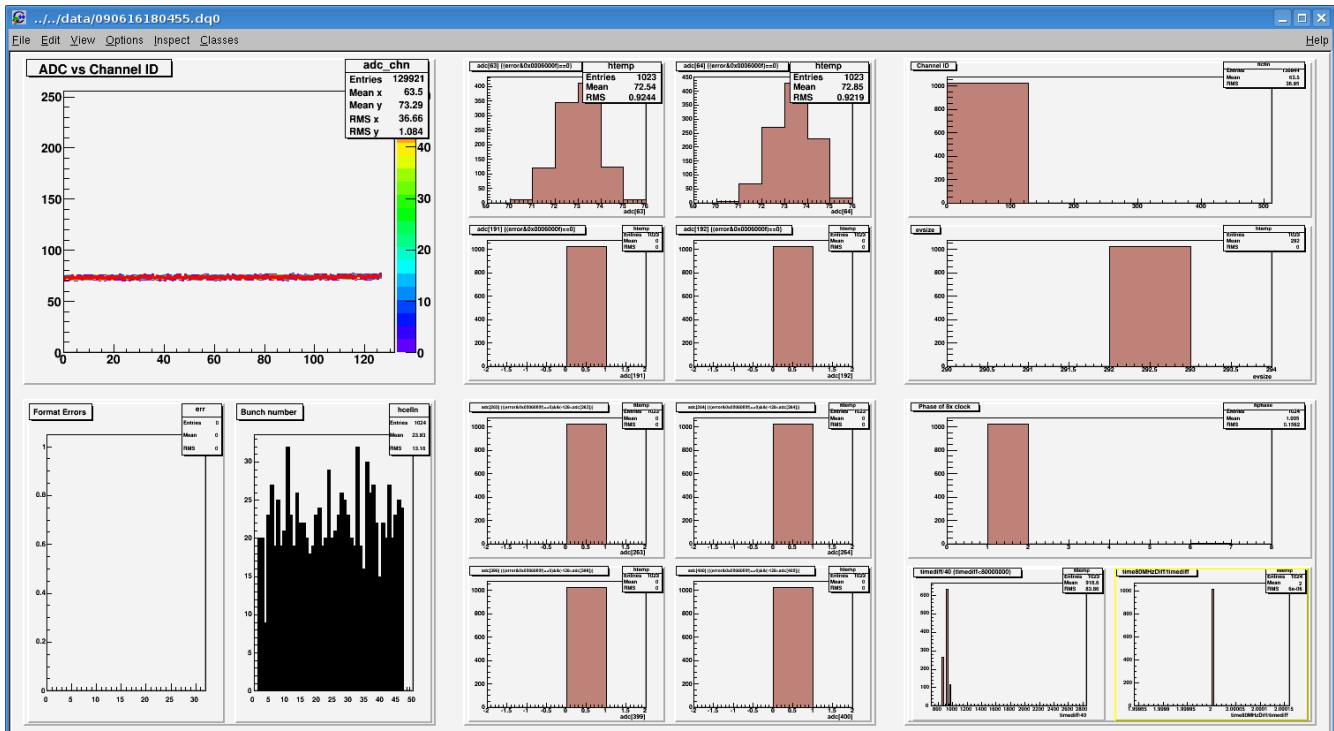


Fig. 3: Test module #2, QuasyD0 mode (FEClk is off during digitization)

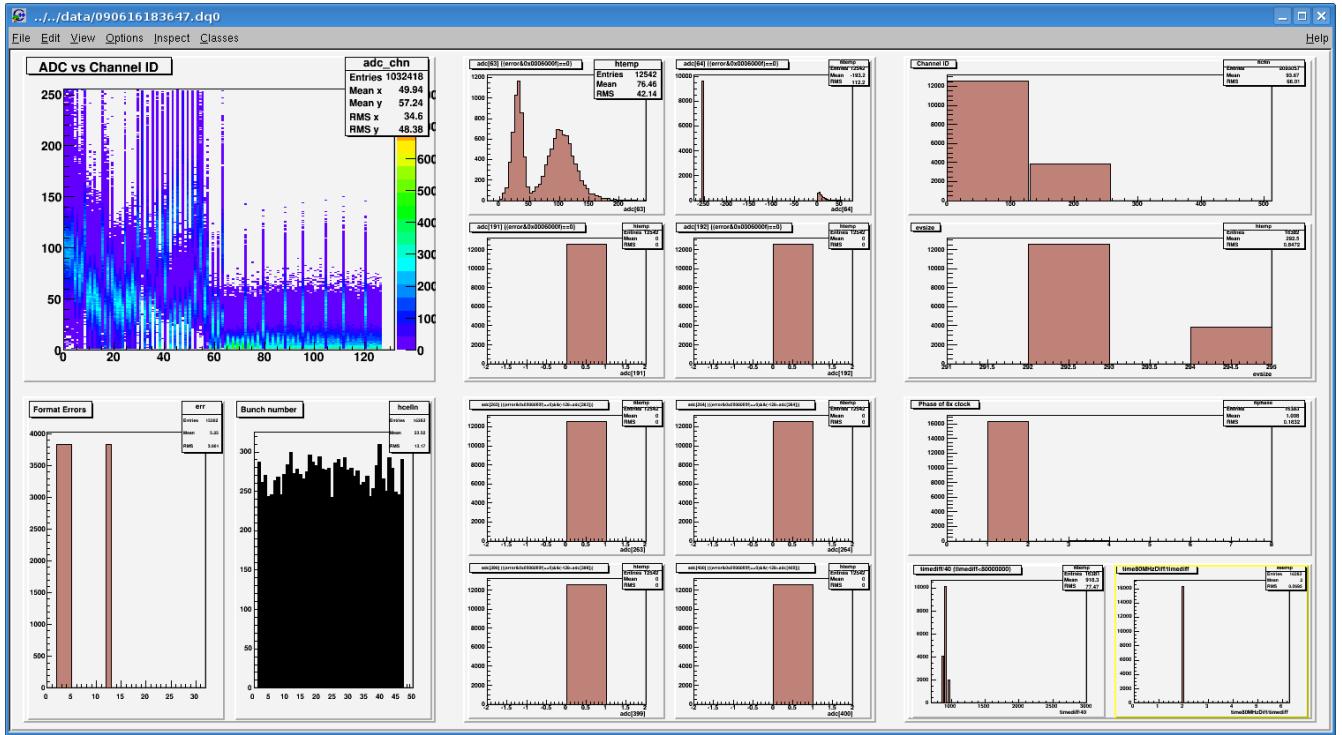


Fig. 4: Good module 432. Lights on.

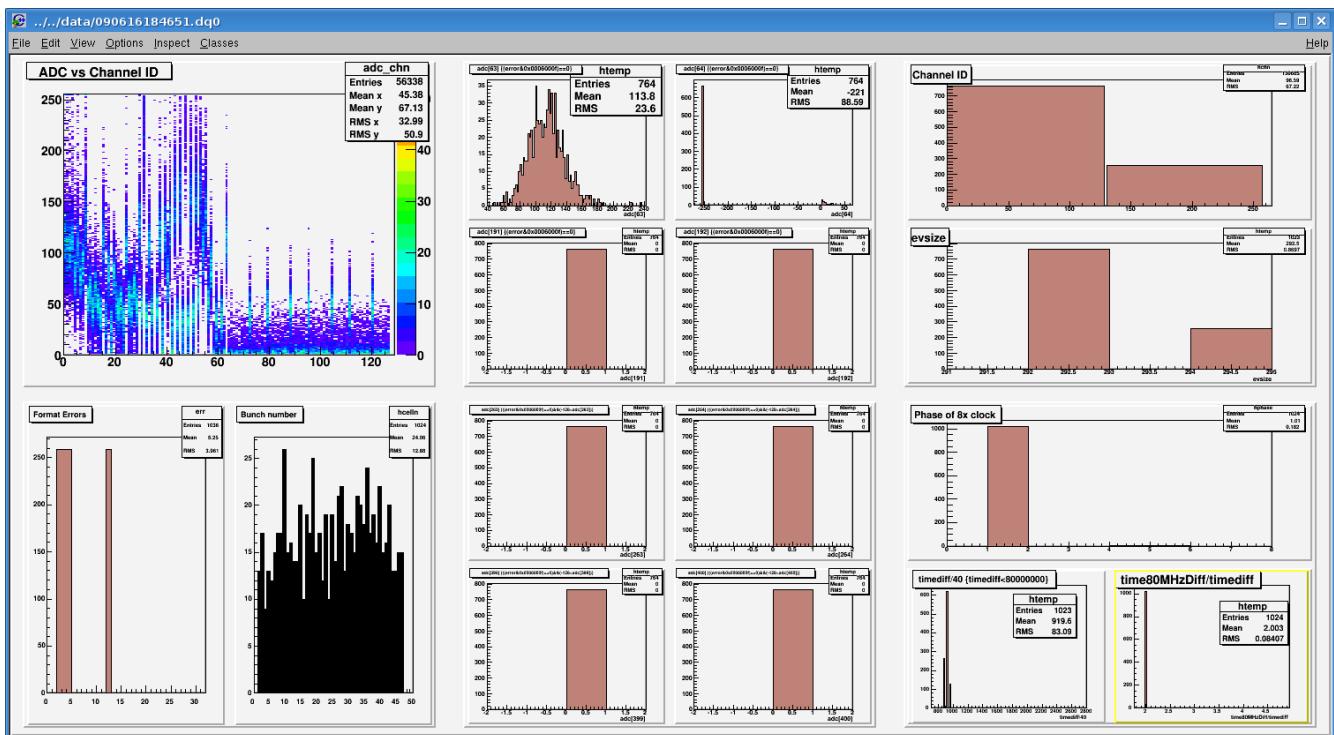


Fig. 5: Good module 432. Light off.

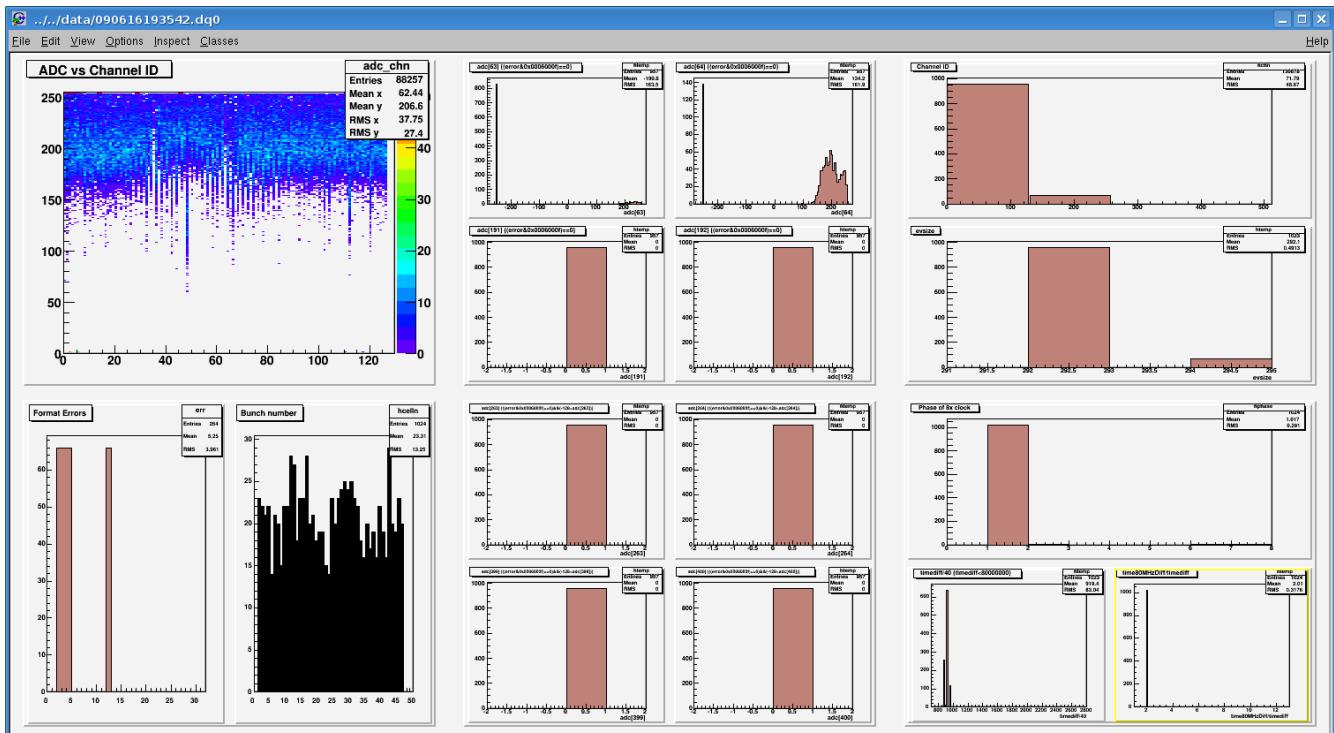
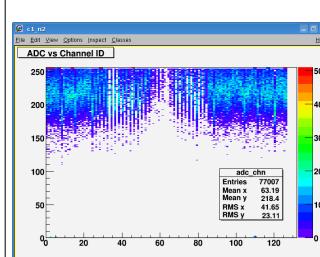
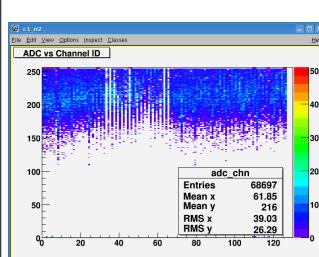


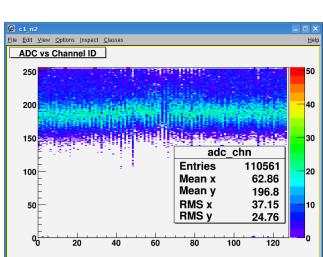
Fig. 6: Module #10 (all channels attached), HV=0



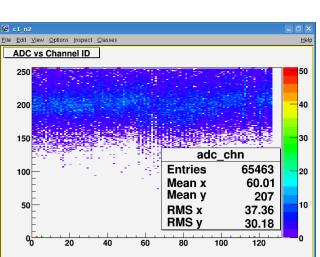
*Fig. 7: Module #10,
Bias=-20V,
Ibias=0.5uA*



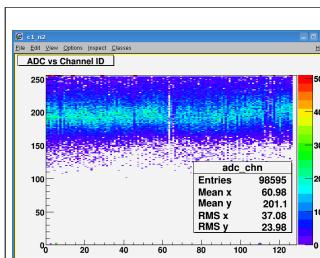
*Fig. 8: Bias=-40V,
Ibias = 0.67uA*



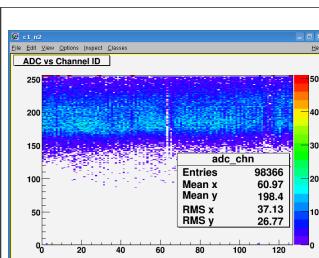
*Fig. 9: Bias = 0, latency
changed from 5 to 6.
The response to the
calibration is worse but
the pickup is much less.*



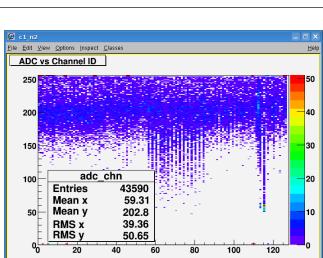
*Fig. 10: Bias -40V,
700nA, Latency 3.*



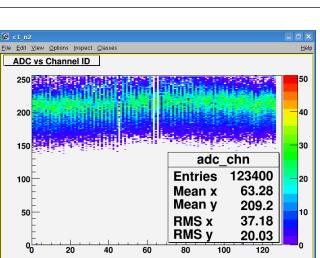
*Fig. 11: Bias -40V
680nA, Latency =1.*



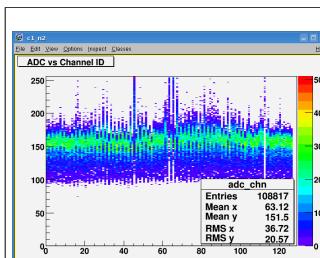
*Fig. 12: Bias -40V,
657nA, Latency 6*



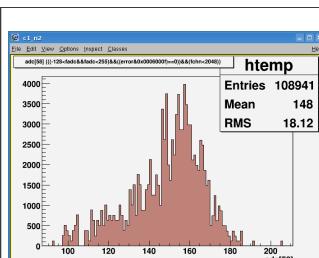
*Fig. 13: Bias -40V,
880nA, cover off, more
light and EM noise.*



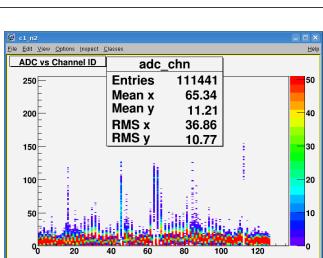
*Fig. 14: Bias -40V,
570nA. Foam cover on.
The previous noise was
due to light.*



*Fig. 15: Bias -40V
570nA, Foam cover.
AGND and DGNA
grounded on SPRC and
on FEM*



*Fig. 16: One channel
#58. RMS = 18*



*Fig. 17: Bias -40V
567nA, Latency 1, RTPS
on.*

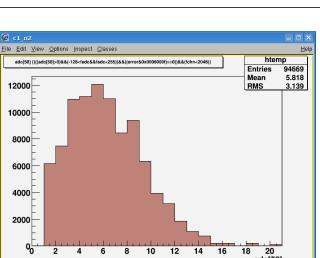


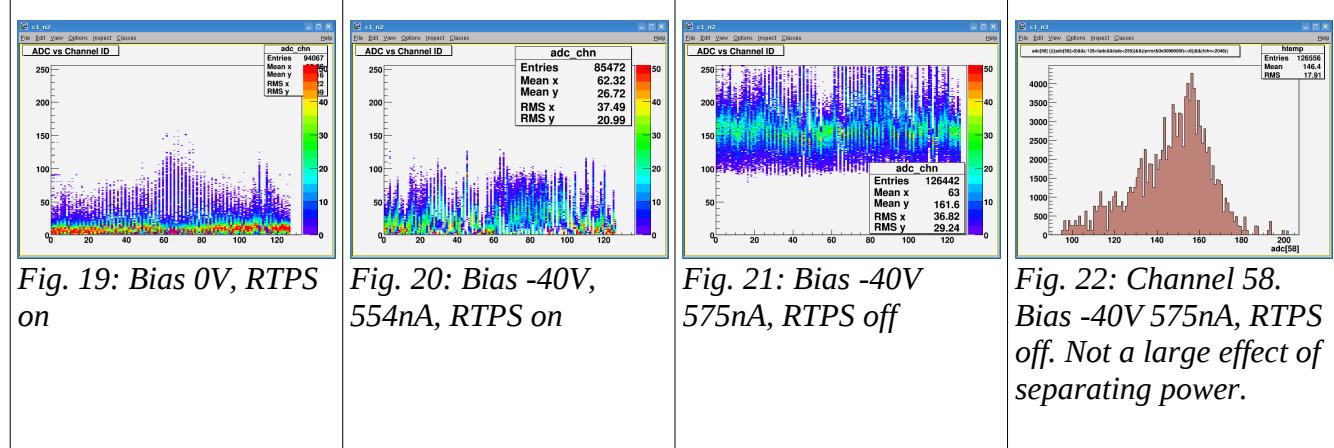
Fig. 18: RTPS On.

AVDD detached from the FEM, AGND disconnected from DGND on the FEM (still connected via inductor).

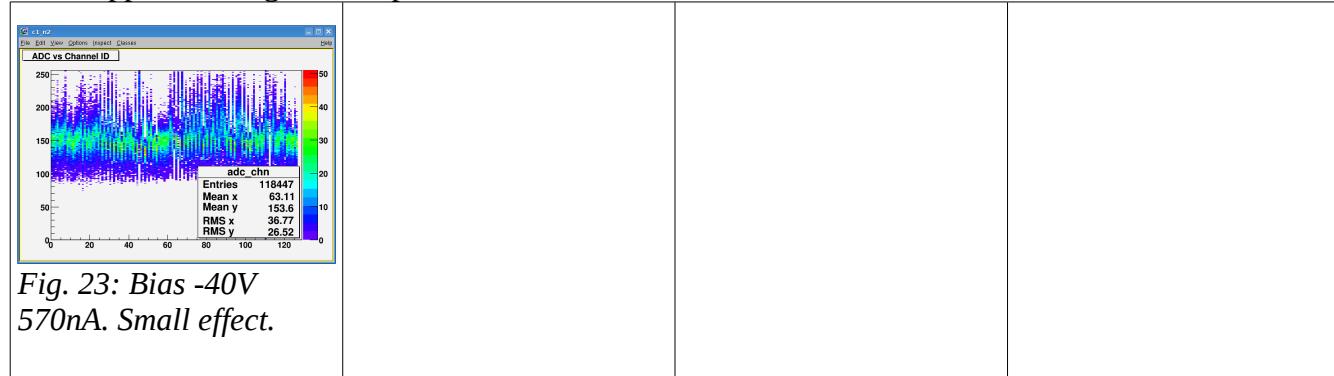
DVDD 5V, 481uA.

After SVX configuration DVDD=0.409, AVDD=2.5V 0.50A

Latency is set to 1 to avoid pickup from CalStrobe (which is at 5th clock)



HV is applied through the stripCar1.



The StripCar1 with module #10 Inside the Enclosure.

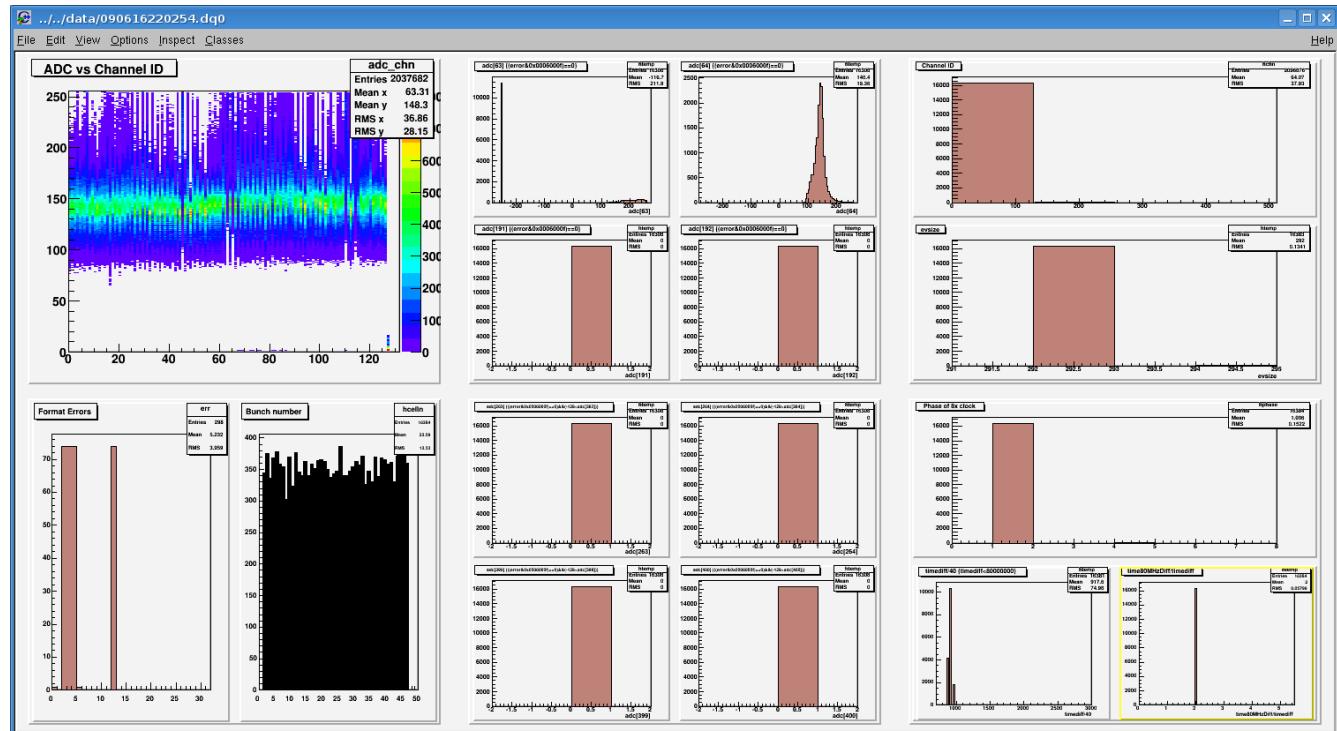


Fig. 24: Bias -40V, 737nA, Latency=1

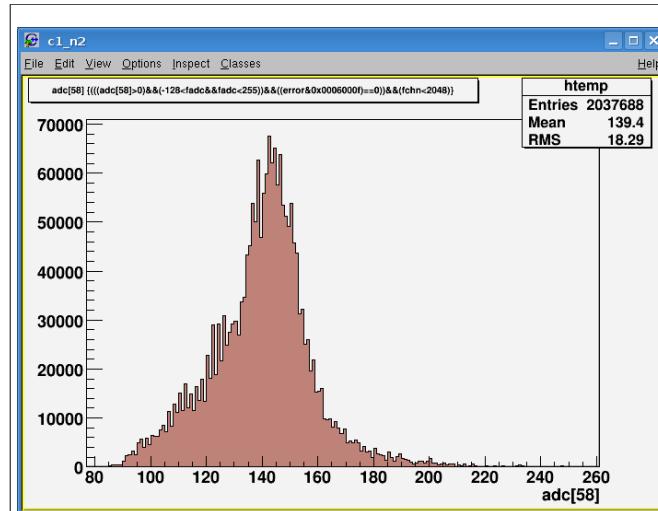


Fig. 25: Channle 58. Bias -40V, 737nA, Latency=1

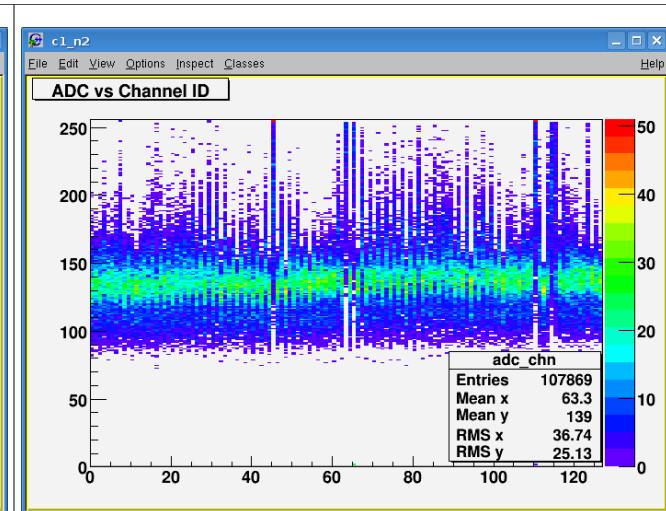


Fig. 26: Latency=3. Two clocks prior the CalStrobe.